Single-Stage LED Driver Based on Coupled Inductor Power Factor Correction and LLC Converter

Alireza Ramezan Ghanbari [1], Sayed Reza Afzali Arani [1], Heinz Seyringer [1], Dietmar Klien [2], Lukas Saccavini [2], Norbert Linder [2]

[1] V-Research, Austria
[2] Tridonic, Austria

Corresponding author and speaker: Alireza Ramezan Ghanbari, alireza.ghanbari@v-research.at

Abstract

In this paper, a single-stage LED driver using coupled inductors for power factor correction (PFC) is presented. The coupled inductors are utilized to charge and discharge the input inductor in each switching cycle, aiming to achieve an ohmic mains behavior result in a high power factor. The conditions of the ohmic mains behavior are analyzed. The coupled inductors are integrated into a half-bridge resonant LLC converter. The driver is designed so that the bus voltage is limited to the reflected secondary voltage, achieving a high power factor while keeping the bus voltage at an applicable level. Additionally, soft switching is achieved during PFC operation. The accuracy of the analytically determined PFC operation is investigated and approved by the experimental results.

1 Introduction

Along with the growing use of LEDs in several lighting systems due to their high efficiency and long lifetime, the requirements and performance of the LED driver, which is an interface between LEDs and power line, are becoming increasingly important [1].

To meet standards such as IEC 61000-3-2, power factor correction (PFC) converters are used in the LED driver industry [2]. Earlier methods for improving the power factor (PF) suggested applying an AC–DC input current shaper converter and a DC–DC converter for regulating the output. A bulk capacitor is applied between the two stages to buffer the input power. This method requires two independent power stages and controllers, so the topology and control become complicated, especially for low power applications, resulting in higher size and price [3]-[4].

Integrating two stages into a single-stage by sharing components, especially switches, leads to a single-stage LED structure that has fewer components and less complexity [5]-[18]. In recent years, this structure has attracted considerable attention. Many studies have focused on integrating the flyback converter with Boost, Buck, Sepic, and resonant converters due to the fewer circuit elements and simplicity of the circuit [6]-[9]. Although single-stage LED drivers using a flyback converter featuring only one switch, the stresses on the switch are relatively high, which limits this type of LED driver for low power applications.

Other studies integrate half-bridge LLC resonant converter with a Boost converter [10]-[18]. The LLC switches inherently provide soft switching which enhances efficiency. This topology achieves low total harmonic distortion (THD) and electromagnetic Interference (EMI) with good efficiency, but the bus voltage is usually twice of the peak of the input voltage, which is impractical for industrial applications.

In [13] to reduce the bus voltage, a hybrid pulse frequency modulation – asymmetric pulse width modulation (PFM-APWM) strategy is proposed. However, the method has complexity in control and results in asymmetric LLC resonant and output diodes currents, impacting efficiency. By using PFM-APWM hybrid control in interleaved Boost stage and full bridge LLC the asymmetric problem can be resolved. Nevertheless, this topology is not well-suited for low power applications [14]. Some studies proposed using interleaved Boost [15]-[16], Buck-Boost [17] and two Boost [18] converters with LLC converters. However, these topologies require large bulk capacitor or have EMI and THD problems. Coupled inductor as a current shaper has been utilized in various studies. In [19], achieving high PF is due to the DCM operation of the coupled inductors inside the dual buck-boost converter sub-circuit,

which is integrated with the LLC resonant converter. However, it suffers from the drawback of high voltage across the bulk capacitor. Utilizing coupled inductors on the AC side of PFC converters may enhance PF. However, challenges like zero crossing and THD persist, and achieving ohmic mains behavior remains unclaimed by existing solutions [20]-[21].

To achieve low THD and EMI, as well as minimize both the bulk capacitor value and the bus voltage while incorporating dimming and maximizing the efficiency, this paper proposes a single-stage LED driver which integrates the coupled inductor PFC with the half-bridge resonant LLC converter.

2 The proposed topology

The proposed single-stage LED driver illustrated in Fig. 1 integrates a half-bridge LLC resonant converter with a coupled inductor to provide power factor correction. The driver is consisting of the coupled inductors L_{C1}, L_{C2} and L_{C3}, input buffer inductor L_f, input rectifier diodes D_1-D_4, two power switches S_1 and S_2 two bulk capacitors C_{b1} and C_{b2}, a resonant network consisting of C_r and L_r, a transformer T_r, output rectifier and a capacitor C_O along with LEDs. The proposed driver eliminates one power switch, one diode and PFC controller in comparison to the conventional two-stage LED driver. The important waveforms are shown in Fig. 2. As can be seen, inductor L_{C1} is periodically charged and discharged by the voltage across C_{b1} and C_{b2} which is $V_{bus}/2$ when switches S_1 and S_2 are turned on respectively. When S_1 is turned on, the voltage across L_{C1} becomes $-V_{bus}/2$. Due to the coupling the voltages across L_{C2} and L_{C3} become $-n_{C2}V_{bus}/2$ and $-n_{C3}V_{bus}/2$, respectively. In the condition where the sum of the input voltage and L_{C2} and L_{C3} voltages exceeds V_{bus}, a surge of input current is supplied to C_{b1} and C_{b2}. When S_2 is turned on, the voltage across L_{C1} becomes $V_{bus}/2$ and the voltages across L_{C2} and L_{C3} are $n_{C2}V_{bus}/2$ and $n_{C3}V_{bus}/2$, respectively. This condition results in L_f discharge. It will be demonstrated that the proposed topology can achieve PFC under specific conditions. The voltage across bulk capacitors is minimally higher than the input voltage and will be clamped to the reflected output voltage under light load condition.

2.1 Operation Principal

In this section, the theoretical operation of the proposed topology is described. The operation is analyzed during a switching period. Following

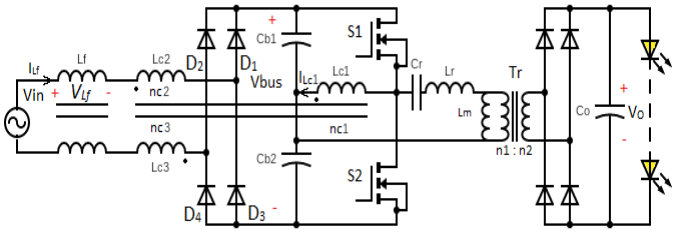

Fig. 1 Proposed single-stage LED driver topology

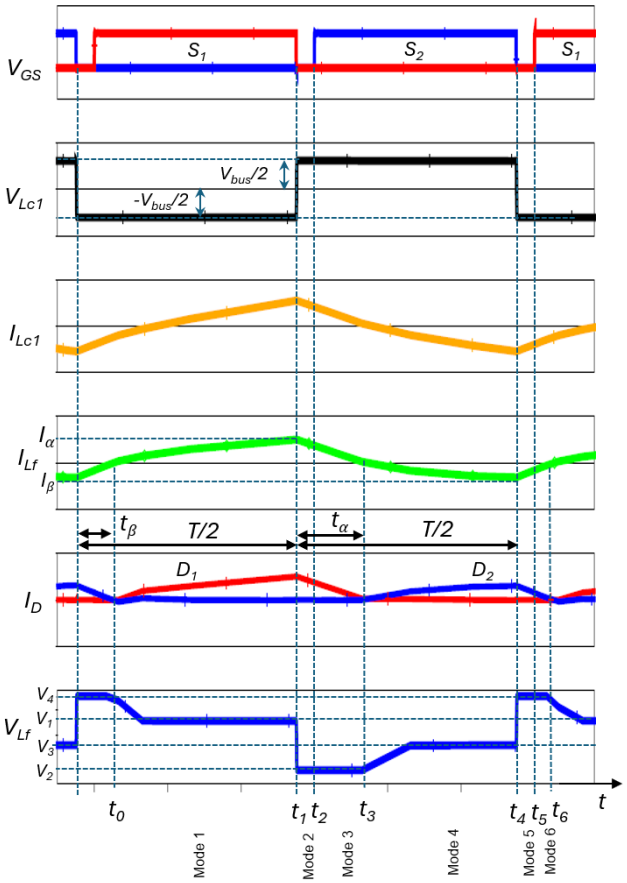

Fig. 2 Important waveforms

assumptions are considered to simplify the converter analysis:

- The input voltage is sinusoidal voltage and considered constant in a switching cycle since the line frequency is significantly lower than the switching frequency.
- The converter operates at steady-state condition.
- The voltage across C_{b1} and C_{b2} is constant throughout an input line cycle.
- The capacitors C_{b1} and C_{b2} have the same value and voltage, considered $V_{bus}/2$.

- The inductors L_{C2} and L_{C3} have the same value and the turn ratios n_{C2} and n_{C3} are equal and considered as n_C.

Mode 1 [$t_0 – t_1$]: At t_0, the switch S_1 is on and the voltage $-V_{bus}/2$ is applied to L_{C1} and to the resonant circuit. In this mode $-n_{C2}V_{bus}/2$ and $-n_{C3}V_{bus}/2$ is applied to L_{C2} and L_{C3} respectively and D_1 and D_4 are conducting. In this mode the voltage across, V_{Lf} is:

$$V_1 = V_{in} + (n_C - 1)V_{bus} \quad (1)$$

So, the L_f current, I_{Lf}, increases almost linearly. At this mode, a resonance occurs via C_{b1}, S_1, L_r, C_r and n_1.

Mode 2 [$t_1 – t_2$]: At t_1 the switch S_1 is turned off and the freewheeling inductor current of converter flows through the body diode of the S_2 and turns it on. The voltage across L_{C1} changes to $V_{bus}/2$ due to S_2 body diode being turned on. In this mode $n_{C2}V_{bus}/2$ and $n_{C3}V_{bus}/2$ is applied to L_{C2} and L_{C3} respectively. I_{Lf} decreases almost linearly while D_1 and D_4 are conducting. Therefore, V_{Lf} is:

$$V_2 = V_{in} - (n_C + 1)V_{bus} \quad (2)$$

Mode 3 [$t_2 – t_3$]: At t_2, S_2 is turned on under zero-voltage switching (ZVS) condition. The voltage $V_{bus}/2$ is applied to L_{C1} and to the resonant circuit. In this mode, another resonance occurs via C_{b2}, S_2, L_r, C_r and n_1 in the reverse direction. The voltage across L_f in this mode is the same as mode 2 and I_{Lf} decreases almost linearly. This mode ends when I_{Lf} reaches zero at t_3.

Mode 4 [$t_3 – t_4$]: At the beginning of this mode, I_{Lf} reaches zero and continues to decrease in the reverse direction. Consequently, D_2 and D_3 start to conduct. The voltage across L_{C1} is still $V_{bus}/2$ and V_{Lf} is:

$$V_3 = V_{in} - (n_C - 1)V_{bus} \quad (3)$$

Mode 5 [$t_4 – t_5$]: At t_4 the switch S_2 is turned off and the voltage across L_{C1} changes to $-V_{bus}/2$ due to S_1 body diode turned on. In this mode $-n_{C2}V_{bus}/2$ and $-n_{C3}V_{bus}/2$ is applied to L_{C2} and L_{C3} respectively and D_2 and D_3 are conducting. In this mode I_{Lf} increases almost linearly and V_{Lf} is:

$$V_4 = V_{in} + (n_C + 1)V_{bus} \quad (4)$$

Mode 6 [$t_5 – t_6$]: At t_5, S_1 is turned on under ZVS condition. The voltage $V_{bus}/2$ is applied to L_{C1} and to the resonant circuit. The voltage across L_f in this mode is the same as mode 5 and I_{Lf} decreases almost linearly. This mode ends when L_f reaches zero at t_6.

2.2 Analysis

In the following, an analysis of the proposed single-stage converter is outlined, along with a discussion of the design procedure for its elements. As shown in Fig. 2, the values of I_α and I_β, representing I_{Lf} positive and negative peaks, are calculated based on V_{Lf} voltage states as:

$$I_\alpha = \frac{V_2}{L_f}t_\alpha = \frac{V_1}{L_f}\left(\frac{T}{2} - t_\beta\right) \quad (5)$$

$$I_\beta = \frac{V_4}{L_f}t_\beta = \frac{V_3}{L_f}\left(\frac{T}{2} - t_\alpha\right) \quad (6)$$

From (5) and (6), t_α and t_β can be calculated as follows.

$$t_\alpha = \frac{V_1}{V_2}\left(\frac{T}{2} - t_\beta\right) \quad (7)$$

$$t_\beta = \frac{V_3}{V_4}\left(\frac{T}{2} - t_\alpha\right) \quad (8)$$

Substituting (8) in (7), the following equation is obtained.

$$t_\alpha = \omega\frac{T}{2}\left(\frac{1-\gamma}{1-\omega\gamma}\right) \quad (9)$$

$$t_\beta = \gamma\frac{T}{2}\left(\frac{1-\omega}{1-\omega\gamma}\right) \quad (10)$$

where $\omega = V_1/V_2$ and $\gamma = V_3/V_4$.

Also, by substituting (9) and (10) in (5) and (6), I_α and I_β can be calculated.

$$I_\alpha = \frac{\omega V_2 T}{2L_f}\left(\frac{1-\gamma}{1-\omega\gamma}\right) \quad (11)$$

$$I_\beta = \frac{\gamma V_4 T}{2L_f}\left(\frac{1-\omega}{1-\omega\gamma}\right) \quad (12)$$

The average input current can be calculated from I_α and I_β averages.

$$I_{Lf,avg} = I_{\alpha,avg} - I_{\beta,avg} = \frac{I_\alpha}{2T}\left(\frac{T}{2} - t_\beta + t_\alpha\right) - \frac{I_\beta}{2T}\left(\frac{T}{2} - t_\alpha + t_\beta\right) \quad (13)$$

Substituting (9)-(12) in (13) the following equation is obtained for $I_{Lf,avg}$:

$$I_{Lf,avg} = \frac{n_C T}{4L_f}V_{in} \quad (14)$$

The consideration of the I_α and I_β signs is essential in the calculation of (13). As can be seen from (14), the input impedance of the proposed converter is ohmic, allowing the input current to follow the input voltage without distortion. The PFC

operation is dependent on the presence of I_β which has a negative current. Otherwise, the input current may experience distortion.

2.3 Design Consideration

The aim is to design an LED driver with PFC capability, regulation, and output dimming. As mentioned before, the proposed driver is the integration of the coupled inductor and the half-bridge resonant LLC converter. The coupled inductors L_{C1}, L_{C2} and L_{C3} are designed to be operated under the condition which provides PFC. The design equation can be expressed as follows. From (1) and (3) and considering V_{in} as a sinusoidal voltage source, the second term of (1) and (3) must be higher than zero [22]. This implies that the n_C must be higher than one.

To limit the current ripple in L_{C1} (ΔI_{Lc1}) which contributes to the conduction and core losses. The value of L_{C1} is calculated as:

$$L_{C1} = \frac{V_{bus} D T_{S,max}}{2\Delta I_{Lc1}} \tag{15}$$

where $T_{S,max}$ is maximum switching period which is related to the minimum switching frequency.

The half-bridge LLC resonant converter is designed to operate across the resonance frequency, providing a wide bus voltage range and dimming capability. According to fundamental harmonic analysis [23], the primary equivalent loads, R_{ac} is:

$$R_{ac} = \frac{8n^2 R_0}{\pi^2} \tag{16}$$

Where R_0 is the LED array equivalent resistance and n is the transformer turn ratio.

The resonant capacitor C_r can be calculated as:

$$C_r = \frac{1}{2\pi f_{rh} R_{ac} Q_r} \tag{17}$$

Where f_{rh} is the higher resonant frequency and Q_r is the quality factor of the resonant network.

Also, the resonant and magnetizing inductors are calculated as follows:

$$L_r = \frac{1}{4\pi^2 f_{rh}^2 C_r} \tag{18}$$

$$L_m = \frac{1}{4\pi^2 f_{rl}^2 C_r} - L_r \tag{19}$$

Where L_m is the magnetizing inductance of the transformer and f_{rl} is the lower resonant frequency. To balance efficiency and regulation m, defined as $(L_m + L_r)/L_r$, is set to 6. The switching frequency range is 55 kHz to 140 kHz.

The bulk capacitors are equal and calculated as:

$$C_{b1,2} = \frac{P_O}{\pi f_{line} V_{bus} \Delta V_{bus}} \tag{20}$$

3 Experimental Results

To validate the theoretical analysis, a universal input, 60 W prototype is manufactured. Table 1 shows the specification and main components of the proposed topology. The coupled inductor currents I_{LC1} and the buffer inductor current I_{Lf1} waveforms as well as the gate-source and drain-source voltages of the S_2 are shown in Fig. 3. As shown, L_{C1} and L_f are continuously charged and discharged to provide the PFC operation. The ZVS is achieved, enhancing overall efficiency. Fig. 4 shows the experimental results of input voltage and current under the input voltage of 230 V and full-load condition. The pure sinusoidal waveform of input current is achieved. The measured PF is 0.994 and THD is approximately 2%. The comparison in Fig. 5 illustrates the input current harmonics of the proposed LED driver under full load and 230V input voltage against the IEC 61000-3-2 Class-C standard. Each harmonic current is significantly lower than the standard values, aligning with the requirements of IEC 61000-3-2. The bus voltage of the proposed LED driver versus output power variation is shown in Fig. 6. As can be seen, this voltage is lower than 440 V under output power variation. The efficency of the manufactured propsed LED driver is shown in Fig. 7.

Component	Designators	Value or part
Input voltage	V_{in}	230 V_{rms}
Output voltage	V_O	48 V
Output current	I_O	1250 mA
Diodes	D_1 - D_4	ES3J
Power Switches	S_1 and S_2	STD10N60M2
Coupled Inductor	L_{C1}, L_{C2} and L_{C3}	700 µH, 1400 µH
Bulk Capacitor	C_{b1}, C_{b2}	22 µF/250V
Resonant network	L_m, L_r, C_r, R_{ac}, Q_r	2100 µH, 400 µH, 3.3 nF, 780Ω, 0.4
Resonant frequencies	f_{r1}, f_{r2}	55 kHz, 140 kHz

Table 1 Proposed Driver Specification

4 Conclusion

A single-stage LED driver with inherent PFC which integrates a half bridge LLC resonant converter with coupled inductors is proposed. It has been shown that the input impedance of the proposed driver is ohmic, enabling the input current to track the input voltage without distortion. The proposed driver bus voltage is not high and is limited to the reflected secondary voltage. The experimental results from the manufactured driver illustrate the attainment of high PF, low THD and ZVS.

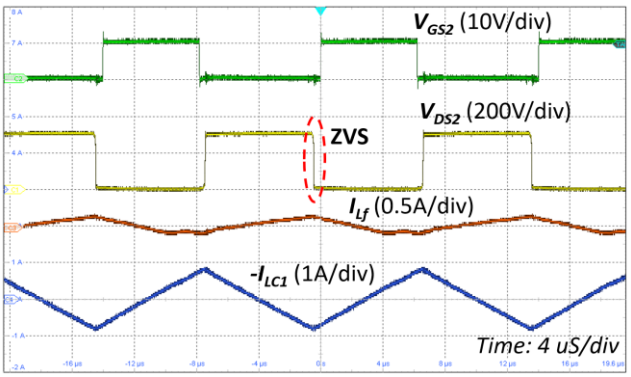

Fig. 3 Switching waveforms

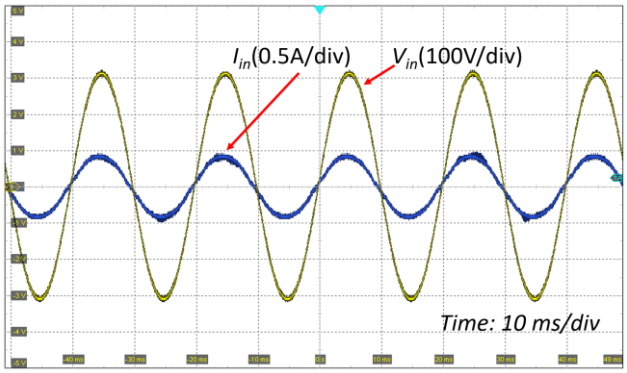

Fig. 4 Input Voltage and Current Waveforms

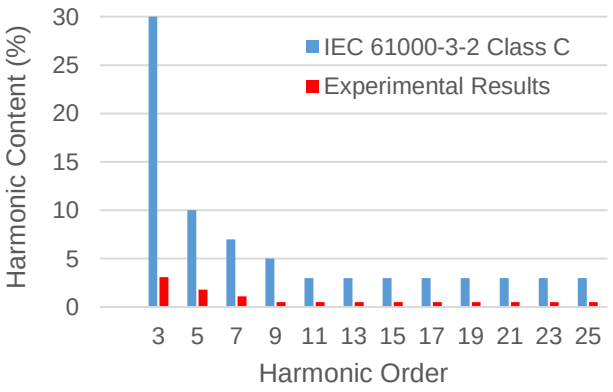

Fig. 5 Input current harmonics at 230V and full load

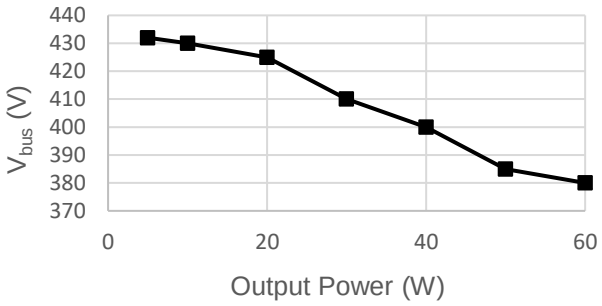

Fig. 6 Bus voltage VS output power

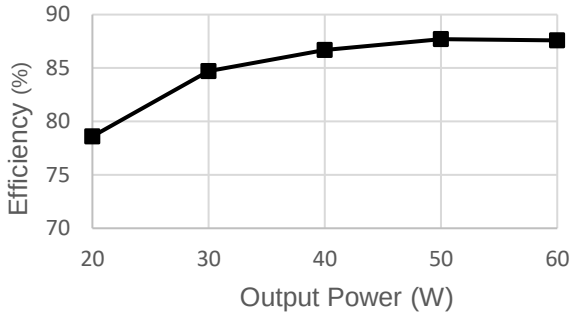

Fig. 7 The measured efficiency VS output power

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